Electronic Circuits

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Digital devices

- Introduction
- Gate characteristics
- Logic families
- TTL
- CMOS
- Interfacing
- Noise and EMC in digital systems.

Introduction

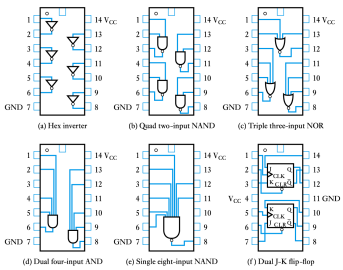
- Earlier we looked at a range of digital applications based on logic gates – at that time we treated the gates as 'black boxes'.
- We will now consider the construction of such gates, and their characteristics.
- Many terms are used to describe **integration level.**
- In this lecture we will concentrate on **small-** and **medium-scale integration circuits** containing just a handful of gates.

Introduction (contd.)

Integration level	Number of transistors
Zero scale integration (ZSI)	1
Small scale integration (SSI)	2–30
Medium scale integration (MSI)	30 - 10^3
Large scale integration (LSI)	10^3 - 10^5
Very large scale integration (VLSI)	10^5 – 10^7
Ultra large scale integration (ULSI)	10^7 – 10^9
Giga-scale integration (GSI)	10^9 – 10^{11}
Tera-scale integration (TSI)	10^{11} – 10^{13}

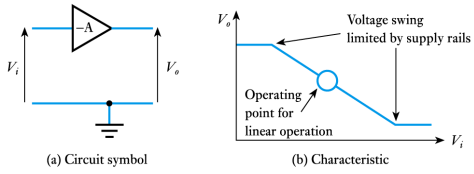
Introduction (contd.)

- **Typical logic device pin-outs.**



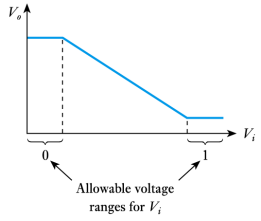
Gate characteristics

- **The inverter or NOT gate**
  - consider the characteristics of a simple inverting amplifier as shown below
  - we normally use only the **linear region.**



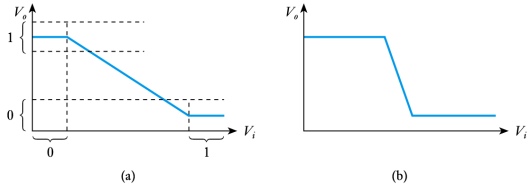
Gate characteristics (contd.)

- We can use an inverting amplifier as a logical inverter but using only the **non-linear** region.



Gate characteristics (contd.)

- We choose input values to ensure that we are always outside of the linear region – as in (a).
- Unlike linear amplifiers, we use circuits with a rapid transition between the non-linear regions – as in (b).



Gate characteristics (contd.)

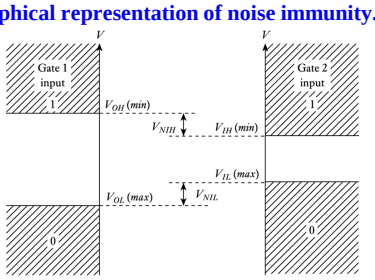
- **Logic levels**
  - The voltage ranges representing '0' and '1' represent the **logic levels** of the circuit.
  - Often **logic 0** is represented by a voltage close to 0 V but the allowable voltage range varies considerably.
  - The voltage used to represent **logic 1** also varies greatly. In some circuits it might be 2-4 V, while in others it might be 12-15 V.
  - In order for one gate to work with another the logic levels must be compatible.

Gate characteristics (contd.)

- **Noise immunity**
  - Noise is present in all real systems.
  - This adds random fluctuations to voltages representing logic levels.
  - To cope with noise, the voltage ranges defining the logic levels are more tightly constrained at the output of a gate than at the input.
  - Thus small amounts of noise will not affect the circuit.
  - The maximum noise voltage that can be tolerated by a circuit is termed its **noise immunity**, V_{NI}.

Gate characteristics (contd.)

- **A graphical representation of noise immunity.**

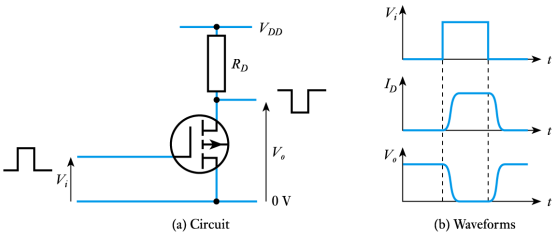


Gate characteristics (contd.)

- **Transistors as switches**
  - Both FETs and bipolar transistors make good switches.
  - Neither form produce *ideal* switches and their characteristics are slightly different.
  - Both forms of device take a finite time to switch and this produces a slight delay in the operation of the gate.
  - This is termed the **propagation delay** of the circuit.

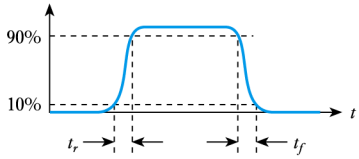
Gate characteristics (contd.)

- **The FET as a logical switch**



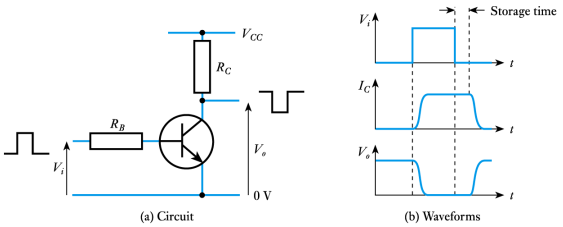
Gate characteristics (contd.)

- **Rise and fall times**
  - because the waveforms are not perfectly square we need a way of measuring switching times
  - we measure the **rise time**, t_r and **fall time**, t_f as shown below



Gate characteristics (contd.)

- **The bipolar transistor as a logical switch**

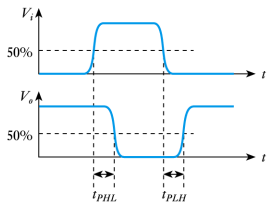


Gate characteristics (contd.)

- When the input voltage to a bipolar transistor is high the transistor turns ON and the output voltage is driven down to its **saturation voltage,** which is about 0.1 V.
- However, saturation of the transistor results in the storage of excess charge in the base region.
- This increases the time taken to turn OFF the device – an effect known as **storage time.**
- This makes the device faster to turn ON than OFF.
- Some switching circuits increase speed by preventing the transistors from entering saturation.

Gate characteristics (contd.)

- **Timing considerations**
  - all gates have a certain **propagation delay time**, t_{PD}
  - this is the average of the two switching times.



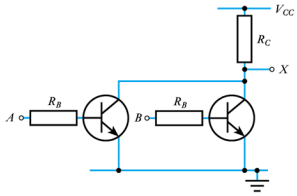
$$t_{PD} = \frac{1}{2}(t_{PHL} + t_{PLH})$$

Logic families

- We have seen that different devices use different voltages ranges for their logic levels.
- They also differ in other characteristics.
- In order to assure correct operation when gates are interconnected they are normally produced in families.
- We will look briefly at a range of logic families, then concentrate on the most important ones, namely **TTL** and **CMOS.**

Logic families (contd.)

- **Resistor-transistor logic (RTL)**
  - an RTL NOR gate

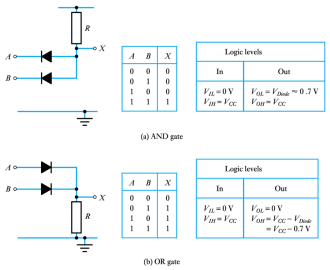


A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

Logic levels
$V_L = V_{CE(sat)} \approx 0.1$ V $V_H = V_{CC}$

Logic families (contd.)

- **Diode logic**



A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

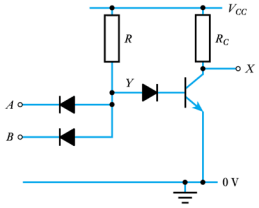
Logic levels	
In	Out
$V_{IL} = 0$ V $V_{IH} = V_{CC}$	$V_{OL} = V_{Diode} \approx 0.7$ V $V_{OH} = V_{CC}$

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

Logic levels	
In	Out
$V_{IL} = 0$ V $V_{IH} = V_{CC}$	$V_{OL} = 0$ V $V_{OH} = V_{CC} - V_{Diode}$ $= V_{CC} - 0.7$ V

Logic families (contd.)

- **Diode-transistor logic**
  - A DTL NAND gate

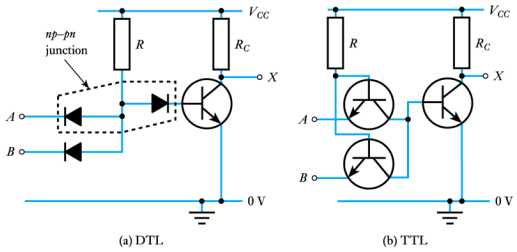


A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

Logic levels
$V_L = V_{CE(sat)} \approx 0.1$ V $V_H = V_{CC}$

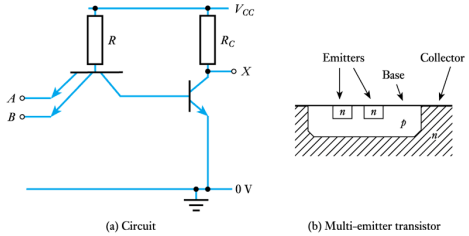
Logic families (contd.)

- Replacing the diodes of a DTL gate with transistors



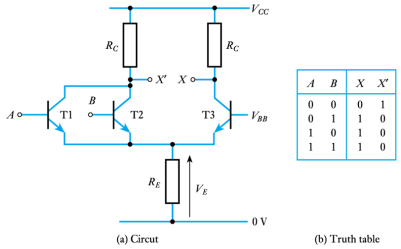
Logic families (contd.)

- **Transistor-transistor logic (TTL)**
  - a simple TTL NAND gate



Logic families (contd.)

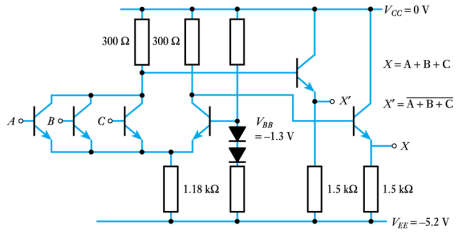
- A non-saturating logic gate.



A	B	X	X′
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

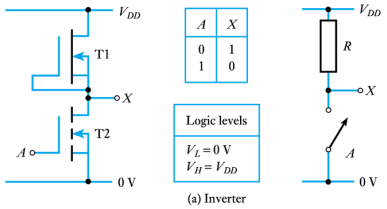
Logic families (contd.)

- **Emitter-coupled logic (ECL)**
  - a three-input ECL OR/NOR gate



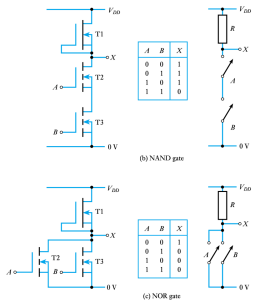
Logic families (contd.)

- **Metal oxide semiconductor (MOS) logic**
  - NMOS gates



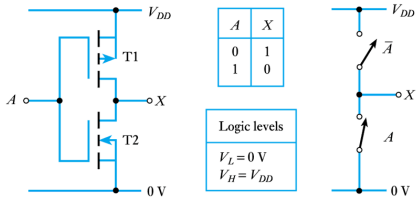
Logic families (contd.)

- NMOS NAND and NOR gates



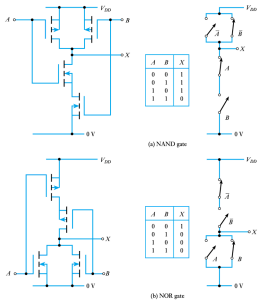
Logic families (contd.)

- **Complementary metal oxide semiconductor (CMOS) logic**
  - a CMOS inverter



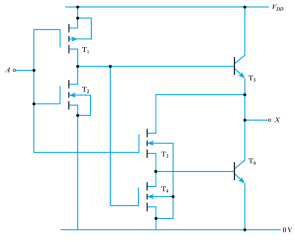
Logic families (contd.)

- two-input CMOS gates



Logic families (contd.)

- **Bipolar CMOS (BiCMOS) logic**
  - a simple BiCMOS inverter

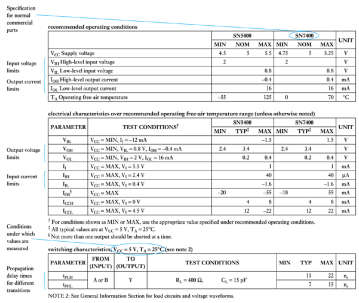


A comparison of logic families

Parameter	TTL	ECL	CMOS
Basic gate	NAND	OR/NOR	NAND-NOR
Fan-out	10	25	>50
Power per gate (mW)	1 – 22	4 – 55	1@1 MHz
Noise immunity	Very good	Good	Excellent
T_{PD} (ns)	l.5 – 33	1 – 4	1.5 – 200

TTL

- **Standard TTL**
  - part of a typical TTL data sheet



recommended operating conditions

	SN5400			SN7400			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5400			SN7400			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		4	8		4	8	mA
I_{CCL}	V_{CC} = MAX, V_I = 4.5 V		12	22		12	22	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

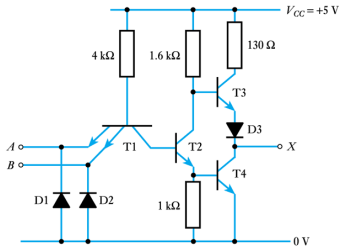
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω, C_L = 15 pF		11	22	ns
t_{PHL}					7	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TTL (contd.)

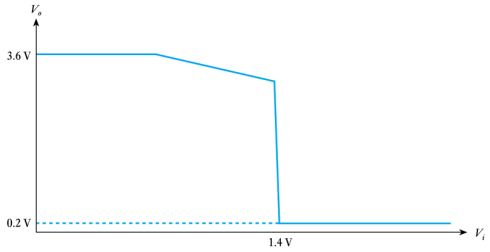
– a TTL two-input NAND gate



A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

TTL (contd.)

– TTL transfer function



TTL (contd.)

– input and output voltage levels for 74 family devices

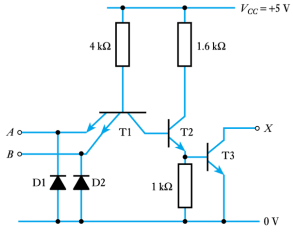
	Minimum	Typical	Maximum
V_{IL}	—	—	0.8
V_{IH}	2.0	—	—
V_{OL}	—	0.2	0.4
V_{OH}	2.4	3.6	—

– **noise immunity in logic 1** (high) V_{NIH} = $V_{OH(min)}$ - $V_{IH(min)}$ = 2.4 – 2.0 = 0.4 V

– **noise immunity in logic 0** (low) V_{NIL} = $V_{IL(max)}$ - $V_{OL(max)}$ = 0.8 – 0.4 = 0.4 V

TTL (contd.)

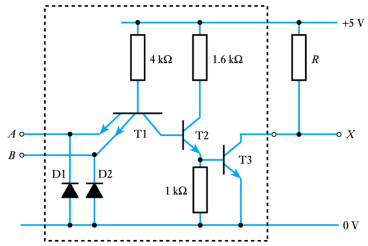
- **Open collector devices**
  - the 7401 two-input NAND gate with open collector output.



A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

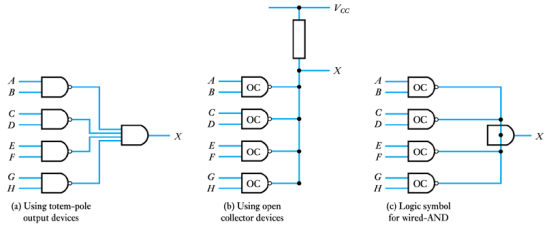
TTL (contd.)

– use of an open collector gate with an external load



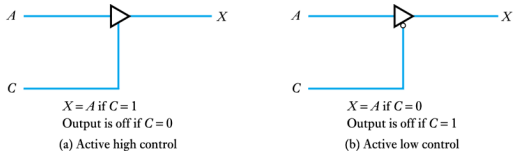
TTL (contd.)

- **Wired-AND operation**



TTL (contd.)

- **Three-state outputs**

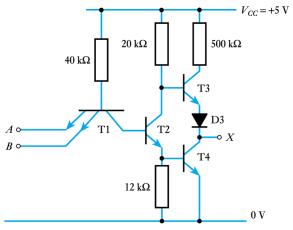


TTL (contd.)

- **TTL inputs**
  - unused inputs, if left unconnected, will float to logical 1
  - it is unadvisable to allow them to float since they are then very susceptible to noise
  - unused inputs should be tied to ground (logic 0) or through a resistor to the positive supply rail (logic 1)
    - unused inputs to an AND or NAND gate should be tied *high*
    - unused inputs to an OR or NOR gate should be tied *low*.

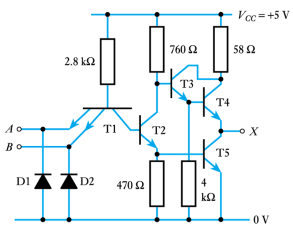
Other TTL families

- **Low-power TTL (74L)**
  - a 74L00 two-input NAND gate



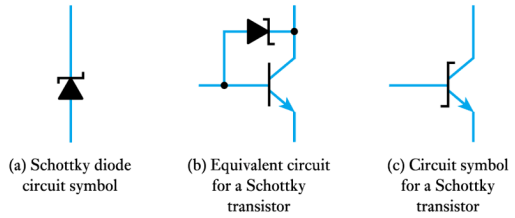
Other TTL families (contd.)

- **High-speed TTL (74H)**
  - a 74H00 two-input NAND gate



Other TTL families (contd.)

- **Schottky TTL (74S)**
  - Schottky diodes and transistors



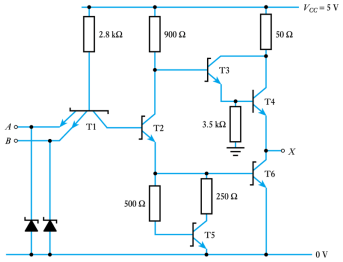
(a) Schottky diode circuit symbol

(b) Equivalent circuit for a Schottky transistor

(c) Circuit symbol for a Schottky transistor

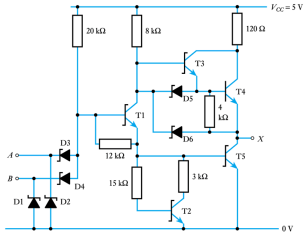
Other TTL families (contd.)

- a 74S00 two-input NAND gate



Other TTL families (contd.)

- **Low-power Schottky TTL (74LS)**
  - a 74LS00 two-input NAND gate

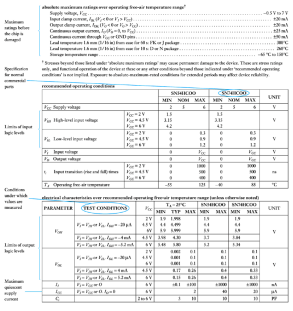


A comparison of TTL families

Family	Descriptor	T_{PD} (ns)	Power per gate (mW)
Standard	74XX	9	10
Low-power	74LXX	33	1
High-speed	74HXX	6	22
Schottky	74SXX	3	19
Advanced Schottky	74ASXX	1.5	8.5
Low-power Schottky	74LSXX	9.5	2
Advanced low-power Schottky	74ALSXX	4	1
FAST	74FXX	2.7	4

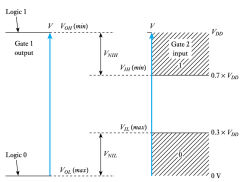
CMOS

- **CMOS**
  - part of a typical CMOS data sheet



CMOS (contd.)

- CMOS input and output voltage levels



- **noise immunity in logic 1** (high) V_{NIH}

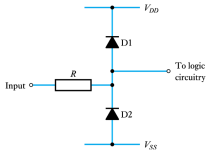
$= V_{OH(min)} - V_{IH(min)}$
$= V_{DD} - 0.7 \times V_{DD}$
$= 0.3 \times V_{DD}$

- **noise immunity in logic 0** (low) $V_{NIL} = V_{IL(max)} - V_{OL(max)}$

$= 0.3 \times V_{DD} - 0$
$= 0.3 \times V_{DD}$

CMOS (contd.)

- **CMOS inputs**
  - CMOS gate protection circuitry



  - CMOS inputs must *not* be left unconnected
  - unused inputs should be tied to ground (logic 0) or to the positive supply rail (logic 1)
    - unused inputs to an AND or NAND gate should be tied *high*
    - unused inputs to an OR or NOR gate should be tied *low.*

CMOS (contd.)

- **CMOS outputs**
  - typical output resistance of about 250Ω (5V operation)
  - high input resistance produces a high fan-out
  - propagation delay increases with the number of gates being driven
  - if high-speed operation is not required, at least 50 gates can be driven from a single output
  - no CMOS equivalent of open-collector output
  - some CMOS gates have three-state facility.

CMOS families

- **Standard CMOS (4000B)**
  - one of the oldest form of CMOS – now largely obsolete
  - operates with supply voltages of 3-18 V
  - can produce very high noise immunity (typically about 0.45 $\times V_{CC}$)
  - relatively slow – propagation delay times of 45–125 ns.

CMOS families (contd.)

- **Standard CMOS with TTL pin-out (74C)**
  - adopts a device numbering scheme compatible with corresponding TTL parts
  - operates with supply voltages of 3–18 V
  - can produce very high noise immunity (typically about 0.45 $\times V_{CC}$)
  - relatively slow – propagation delay times of 30–50 ns.

CMOS families (contd.)

- **High-speed CMOS (74HC)**
  - will operate with supply voltages of 2–6 V, but often uses a 5 V supply
  - significantly faster than standard CMOS ($T_{PD} \approx$ 8ns)
- **High-speed CMOS, TTL compatible inputs (74HCT)**
  - another high-speed family, which offers TTL compatible inputs
  - operates with supply voltages of 4.5–5.5 V
  - direct replacements for similar TTL parts, with similar speeds to 74LS parts.

CMOS families (contd.)

- **Advanced CMOS (74AC)**
  - offer a significant speed advantage over high-speed CMOS ($T_{PD} \approx$ 4ns), with similar power consumption
  - will operate with supply voltages of 2–6 V
- **Advanced CMOS , TTL compatible inputs (74ACT)**
  - offers similar performance to Advanced CMOS, but has TTL compatible inputs
  - operates with supply voltages of 4.5–5.5 V.

CMOS families (contd.)

- **Low-voltage CMOS (74LV)**
  - can be used with supply voltages of 2 – 5.5 V, permitting low voltage operation where necessary
- **Advanced, low-voltage CMOS (74ALVC)**
  - this advanced low-voltage family can be used with supply voltages between 1.65 and 3.6 V
  - provides considerable speed advantage compared to the 74LV series
  - T_{PD} might be 3 ns when used with a supply voltage of 3.0 V, increasing to 4.4 ns when used at 1.8 V.

CMOS families (contd.)

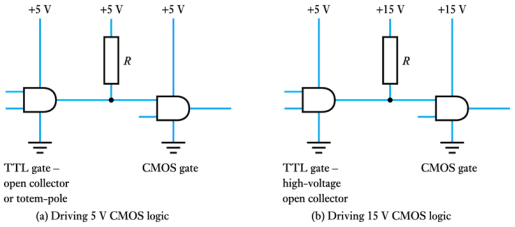
- **BiCMOS (74BCT)**
  - provides a range of high-speed input/output and device driver circuits
  - normally used with a supply voltage of 5 V, but will accept supply voltages in the range 4.5 – 5.5 V
  - typical T_{PD} about 3–4 ns.
- **Low-voltage BiCMOS (74LVT)**
  - offers BiCMOS operation in a family that can be used with supply voltages between 2.7 and 3.6 V.

A comparison of CMOS families

Family	Descriptor	T_{PD} (ns)	Static power per gate (μW)
Standard	4000B	75	50
Standard, TTL pin-out	74CXX	50	50
High-speed	74HCXX	8	25
High-speed, TTL compatible	74HCTXX	12	25
Advanced	74ACXX	4	25
Advanced, TTL compatible	74ACTXX	6	25
Low-voltage	74LVXX	9	50
Advanced, low-voltage	74ALVCXX	3	50
BiCMOS	74BCTXX	3.5	600
Low-voltage BiCMOS	74LVTXX	4	400

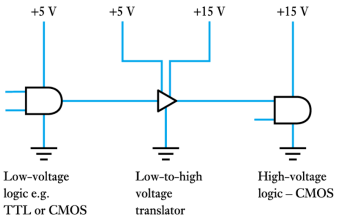
Interfacing TTL and CMOS

- **Driving CMOS from TTL**



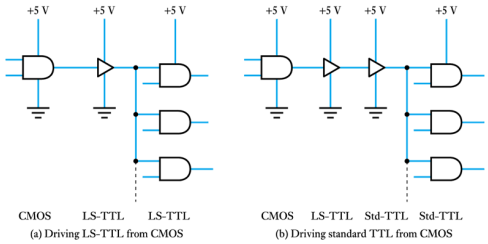
Interfacing TTL and CMOS (contd.)

– use of a low-to-high voltage translator



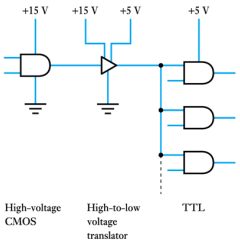
Interfacing TTL and CMOS (contd.)

- **Driving TTL from CMOS**



Interfacing TTL and CMOS (contd.)

– using a high-to-low voltage translator



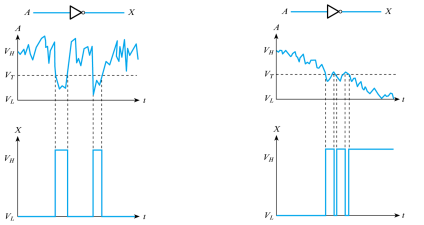
(c) Driving TTL from high-voltage CMOS

Noise and EMC in digital systems

- **Digital noise sources**
  - Electronic noise
  - Interference
  - Internal noise
  - Power supply noise
  - CMOS switching transients.

Noise and EMC in digital systems (contd.)

- **The effects of noise in digital systems**

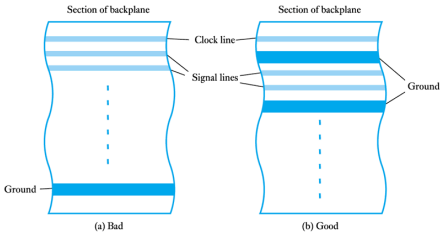


Steady logic voltages

Slowly varying signals

Noise and EMC in digital systems (contd.)

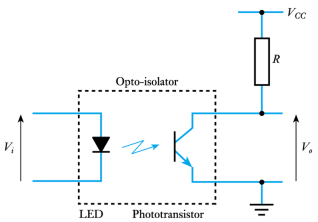
- **Designing digital systems for EMC**
  - backplane arrangements



(a) Bad (b) Good

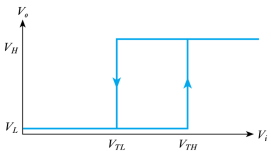
Noise and EMC in digital systems (contd.)

– opto-isolation

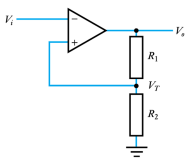


Noise and EMC in digital systems (contd.)

– Schmitt trigger inputs



Transfer characteristics



A simple Schmitt trigger circuit

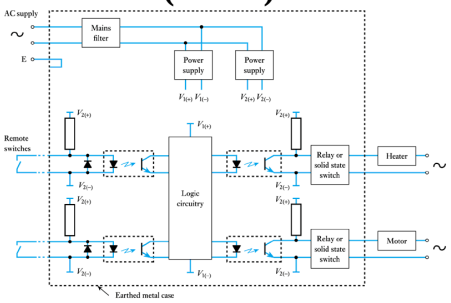
Noise and EMC in digital systems (contd.)

- **A design example**

An industrial control system

A system is connected to **two remote mechanical switches**, and to an **AC heater** and an **AC motor**. The controller is required to take signals from the switches and to turn the heater and motor ON and OFF according to some control algorithm. The system is to be used in an environment with a **high level of electrical noise**. Suggest how the unit could be designed to minimize the effects of noise on its operation.

Noise and EMC in digital systems (contd.)



Key points

- Physical gates are not ideal components.
- Logic gates are manufactured in a range of logic families.
- The ability of a gate to ignore noise is its ‘noise immunity’.
- Both MOSFETs and bipolar transistors are used in gates.
- All logic gates exhibit a propagation delay.
- The most widely used logic families are TTL and CMOS.
- Both TTL and CMOS gates are produced in a range of versions, each optimised for a particular characteristic.
- Interface circuitry may be needed to link devices of different families.
- Noise and EMC issues must be considered during design.