

Electronic Circuits

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Common FET Biasing Circuits

JFET Biasing Circuits

- Fixed – Bias
- Self-Bias
- Voltage-Divider Bias

D-Type MOSFET Biasing Circuits

- Self-Bias
- Voltage-Divider Bias

E-Type MOSFET Biasing Circuits

- Feedback Configuration
- Voltage-Divider Bias

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Basic Current Relationships

For all FETs:

$$I_G \cong 0A$$

$$I_D = I_S$$

For JFETs and D-Type MOSFETs:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

For E-Type MOSFETs:

$$I_D = k(V_{GS} - V_T)^2$$

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Fixed-Bias Configuration

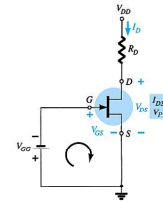
$$V_{DS} = V_{DD} - I_D R_D$$

$$V_S = 0V$$

$$V_C = V_{DS}$$

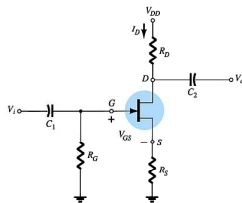
$$V = V_{GS}$$

$$V_{GS} = -V_{GG}$$



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Self-Bias Configuration



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Self-Bias Calculations

For the indicated loop, $V_{GS} = -I_D R_S$

To solve this equation:

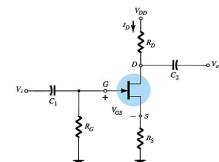
- Select an $I_D < I_{DSS}$ and use the component value of R_S to calculate V_{GS} .
- Plot the point identified by I_D and V_{GS} . Draw a line from the origin of the axis to this point.
- Plot the transfer curve using I_{DSS} and V_P ($V_P = V_{GS(off)}$ in specification sheets) points such as $I_D = I_{DSS}/4$ and $I_D = I_{DS}$.

The Q-point is located where the first line intersects the transfer curve. Use the value of I_D at the Q-point (I_{DQ}) to solve for the other voltages:

$$V_{DS} = V_{DD} - I_D (R_S + R_D)$$

$$V_S = I_D R_S$$

$$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$$

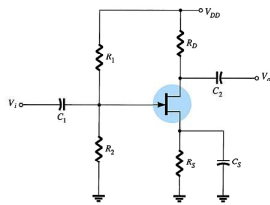


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Voltage-Divider Bias

$I_G = 0 \text{ A}$

I_D responds to changes in V_{GS} .



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Voltage-Divider Bias Calculations

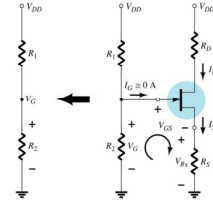
V_G is equal to the voltage across divider resistor R_2 :

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Using Kirchhoff's Law:

$$V_{GS} = V_G - I_D R_S$$

The Q point is established by plotting a line that intersects the transfer curve.



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Voltage-Divider Q-point

Step 1

Plot the line by plotting two points:

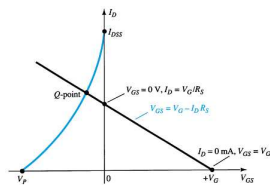
- $V_{GS} = V_G, I_D = 0 \text{ A}$
- $V_{GS} = 0 \text{ V}, I_D = V_G / R_S$

Step 2

Plot the transfer curve by plotting I_{DSS}, V_P and the calculated values of I_D

Step 3

The Q-point is located where the line intersects the transfer curve



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Voltage-Divider Bias Calculations

Using the value of I_D at the Q-point, solve for the other variables in the voltage-divider bias circuit:

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

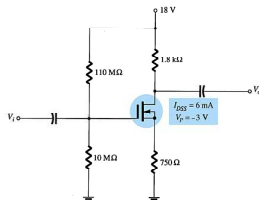
$$V_S = I_D R_S$$

$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

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D-Type MOSFET Bias Circuits

Depletion-type MOSFET bias circuits are similar to those used to bias JFETs. The only difference is that depletion-type MOSFETs can operate with positive values of V_{GS} and with I_D values that exceed I_{DSS} .



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Self-Bias

Step 1

Plot line for

- $V_{GS} = V_G, I_D = 0 \text{ A}$
- $I_D = V_G / R_S, V_{GS} = 0 \text{ V}$

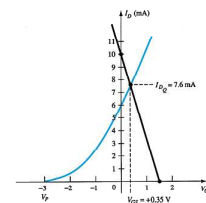
Step 2

Plot the transfer curve using I_{DSS}, V_P and calculated values of I_D

Step 3

The Q-point is located where the line intersects the transfer curve. Use the I_D at the Q-point to solve for the other variables in the voltage-divider bias circuit.

These are the same steps used to analyze JFET self-bias circuits.



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Voltage-Divider Bias

Step 1

Plot the line for

- $V_{GS} = V_G$, $I_D = 0$ A
- $I_D = V_G/R_S$, $V_{GS} = 0$ V

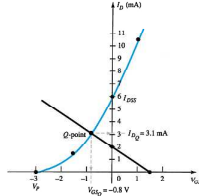
Step 2

Plot the transfer curve using I_{DSS} , V_P and calculated values of I_D .

Step 3

The Q-point is located where the line intersects the transfer curve is. Use the I_D at the Q-point to solve for the other variables in the voltage-divider bias circuit.

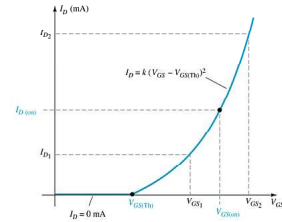
These are the same steps used to analyze JFET voltage-divider bias circuits.



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E-Type MOSFET Bias Circuits

The transfer characteristic for the e-type MOSFET is very different from that of a simple JFET or the d-type MOSFET.



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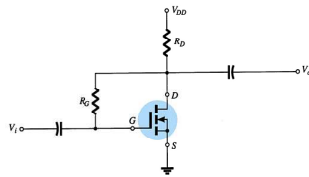
Feedback Bias Circuit

$$I_G = 0 \text{ A}$$

$$V_{RG} = 0 \text{ V}$$

$$V_{DS} = V_{GS}$$

$$V_{GS} = V_{DD} - I_D R_D$$



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Feedback Bias Q-Point

Step 1

Plot the line using

- $V_{GS} = V_{DD}$, $I_D = 0$ A
- $I_D = V_{DD}/R_D$, $V_{GS} = 0$ V

Step 2

Using values from the specification sheet, plot the transfer curve with

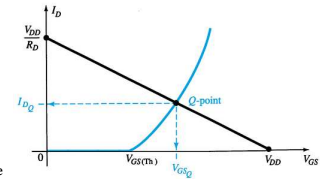
- $V_{GS(th)}$, $I_D = 0$ A
- $V_{GS(on)}$, $I_{D(on)}$

Step 3

The Q-point is located where the line and the transfer curve intersect

Step 4

Using the value of I_D at the Q-point, solve for the other variables in the bias circuit



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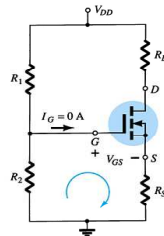
Voltage-Divider Biasing

Plot the line and the transfer curve to find the Q-point. Use these equations:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_S + R_D)$$



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Voltage-Divider Bias Q-Point

Step 1

Plot the line using

- $V_{GS} = V_G = (R_2 V_{DD}) / (R_1 + R_2)$, $I_D = 0$ A
- $I_D = V_G / R_S$, $V_{GS} = 0$ V

Step 2

Using values from the specification sheet, plot the transfer curve with

- $V_{GS(th)}$, $I_D = 0$ A
- $V_{GS(on)}$, $I_{D(on)}$

Step 3

The point where the line and the transfer curve intersect is the Q-point.

Step 4

Using the value of I_D at the Q-point, solve for the other circuit values.

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***p*-Channel FETs**

For *p*-channel FETs the same calculations and graphs are used, except that the voltage polarities and current directions are reversed.

The graphs are mirror images of the *n*-channel graphs.

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Applications

Voltage-controlled resistor
JFET voltmeter
Timer network
Fiber optic circuitry
MOSFET relay driver

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