Electronic Circuits

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FETs vs. BJTs

Similarities:
- Amplifiers
- Switching devices
- Impedance matching circuits

Differences:
- FETs are voltage controlled devices.
- BJTs are current controlled devices.
- FETs have a higher input impedance.
- BJTs have higher gains.
- FETs are less sensitive to temperature variations and are more easily integrated on ICs.
- FETs are generally more static sensitive than BJTs.

FET Types

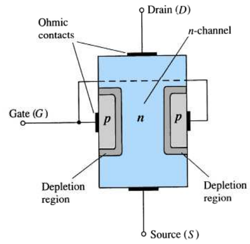
- **JFET:** Junction FET
- **MOSFET:** Metal–Oxide–Semiconductor FET
  - **D-MOSFET:** Depletion MOSFET
  - **E-MOSFET:** Enhancement MOSFET

JFET Construction

There are two types of JFETs

- *n*-channel
- *p*-channel

The n-channel is more widely used.



There are three terminals:

- **Drain** (D) and **Source** (S) are connected to the *n*-channel
- **Gate** (G) is connected to the *p*-type material

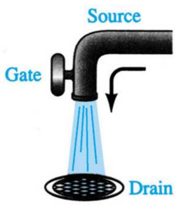
JFET Operation: The Basic Idea

JFET operation can be compared to a water spigot.

The source of water pressure is the accumulation of electrons at the negative pole of the drain-source voltage.

The drain of water is the electron deficiency (or holes) at the positive pole of the applied voltage.

The control of flow of water is the gate voltage that controls the width of the n-channel and, therefore, the flow of charges from source to drain.



JFET Operating Characteristics

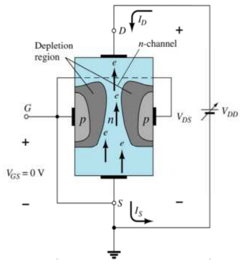
There are three basic operating conditions for a JFET:

- $V_{GS} = 0$, V_{DS} increasing to some positive value
- $V_{GS} < 0$, V_{DS} at some positive value
- Voltage-controlled resistor

JFET Operating Characteristics: V_{GS} = 0 V

Three things happen when V_{GS} = 0 and V_{DS} is increased from 0 to a more positive voltage

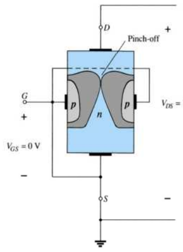
- The depletion region between p-gate and n-channel increases as electrons from n-channel combine with holes from p-gate.
- Increasing the depletion region, decreases the size of the n-channel which increases the resistance of the n-channel.
- Even though the n-channel resistance is increasing, the current (I_D) from source to drain through the n-channel is increasing. This is because V_{DS} is increasing.



JFET Operating Characteristics: Pinch Off

If V_{GS} = 0 and V_{DS} is further increased to a more positive voltage, then the depletion zone gets so large that it pinches off the n-channel.

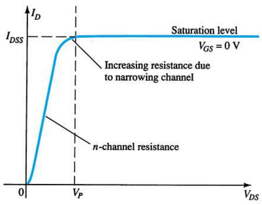
This suggests that the current in the n-channel (I_D) would drop to 0A, but it does just the opposite–as V_{DS} increases, so does I_D.



JFET Operating Characteristics: Saturation

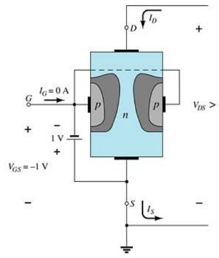
At the pinch-off point:

- Any further increase in V_{GS} does not produce any increase in I_D. V_{GS} at pinch-off is denoted as V_p.
- I_D is at saturation or maximum. It is referred to as I_{DSS}.
- The ohmic value of the channel is maximum.



JFET Operating Characteristics

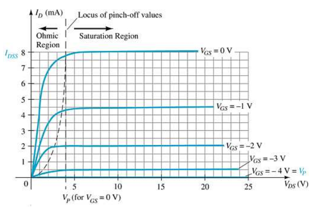
As V_{GS} becomes more negative, the depletion region increases.



JFET Operating Characteristics

As V_{GS} becomes more negative:

- The JFET experiences pinch-off at a lower voltage (V_P).
- I_D decreases ($I_D < I_{DSS}$) even though V_{DS} is increased.
- Eventually I_D reaches 0 A. V_{GS} at this point is called V_p or $V_{GS(off)}$.



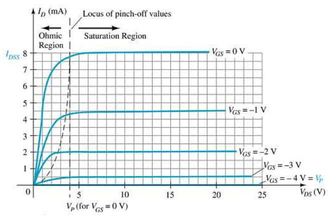
Also note that at high levels of V_{DS} the JFET reaches a breakdown situation. I_D increases uncontrollably if $V_{DS} > V_{DSmax}$.

JFET Operating Characteristics: Voltage-Controlled Resistor

The region to the left of the pinch-off point is called the ohmic region.

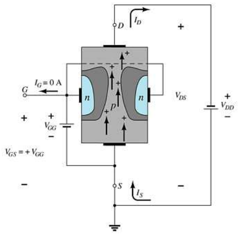
The JFET can be used as a variable resistor, where V_{GS} controls the drain-source resistance (r_d). As V_{GS} becomes more negative, the resistance (r_d) increases.

$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$



p-Channel JFETS

The *p*-channel JFET behaves the same as the *n*-channel JFET, except the voltage polarities and current directions are reversed.



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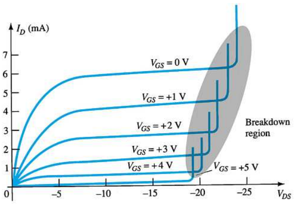
p-Channel JFET Characteristics

As V_{GS} increases more positively

- The depletion zone increases
- I_D decreases ($I_D < I_{DSS}$)
- Eventually $I_D = 0$ A



Also note that at high levels of V_{DS} the JFET reaches a breakdown situation: I_D increases uncontrollably if $V_{DS} > V_{DSmax}$.

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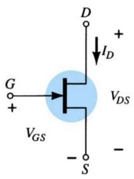
N-Channel JFET Symbol



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JFET Transfer Characteristics

The transfer characteristic of input-to-output is not as straightforward in a JFET as it is in a BJT.

In a BJT, β indicates the relationship between I_B (input) and I_C (output).

In a JFET, the relationship of V_{GS} (input) and I_D (output) is a little more complicated:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

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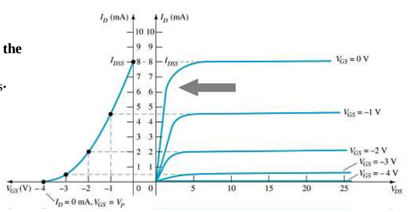
JFET Transfer Curve

This graph shows the value of I_D for a given value of V_{GS}.



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Plotting the JFET Transfer Curve

Using I_{DSS} and Vp ($V_{GS(off)}$) values found in a specification sheet, the transfer curve can be plotted according to these three steps:

Step 1

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Solving for V_{GS} = 0V $\quad I_D = I_{DSS}$

Step 2

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Solving for $V_{GS} = V_p$ ($V_{GS(off)}$) $\quad I_D$ = 0A

Step 3

Solving for V_{GS} = 0V to V_p $\quad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

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JFET Specifications Sheet

Electrical Characteristics

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage ($I_G = -10\ \mu$Adc, $V_{DS} = 0$)		$V_{(BR)GSS}$	-25	–	–	Vdc
Gate Reverse Current ($V_{GS} = -15$ Vdc, $V_{DS} = 0$)		I_{GSS}	–	–	-1.0	nAdc
($V_{GS} = -15$ Vdc, $V_{DS} = 0$, $T_A = 100°C$)			–	–	-200	
Gate Source Cutoff Voltage ($V_{DS} = 15$ Vdc, $I_D = 10$ nAdc)	2N5457	$V_{GS(off)}$	-0.5	–	-6.0	Vdc
Gate Source Voltage ($V_{DS} = 15$ Vdc, $I_D = 100\ \mu$Adc)	2N5457	V_{GS}	–	-2.5	–	Vdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current* ($V_{DS} = 15$ Vdc, $V_{GS} = 0$)	2N5457	I_{DSS}	1.0	3.0	5.0	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance Common Source* ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 kHz)	2N5457	$\lvert y_{fs} \rvert$	1000	–	5000	µmhos
Output Admittance Common Source* ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 kHz)		$\lvert y_{os} \rvert$	–	10	50	µmhos
Input Capacitance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 MHz)		C_{iss}	–	4.5	7.0	pF
Reverse Transfer Capacitance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 MHz)		C_{rss}	–	1.5	3.0	pF

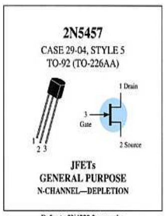
*Pulse Test: Pulse Width ≤ 630 ms; Duty Cycle ≤ 10%

JFET Specifications Sheet

Maximum Ratings

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	V_{GSR}	-25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ $T_A = 25°C$	P_D	310	mW
Derate above 25°C		2.82	mW/°C
Junction Temperature Range	T_J	125	°C
Storage Channel Temperature Range	T_{stg}	-65 to +150	°C



Refer to 2N4220 for graphs.

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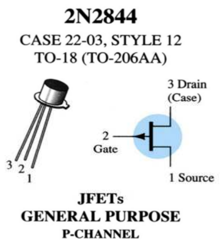
Case and Terminal Identification



Testing JFETs

- **Curve Tracer**
  A curve tracer displays the I_D versus V_{DS} graph for various levels of V_{GS}.
- **Specialized FET Testers**
  These testers show I_{DSS} for the JFET under test.

MOSFETs

MOSFETs have characteristics similar to JFETs and additional characteristics that make then very useful.

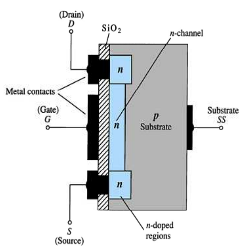
There are two types of MOSFETs:

- Depletion-Type
- Enhancement-Type

Depletion-Type MOSFET Construction

The Drain (D) and Source (S) connect to the to *n*-doped regions. These *n*-doped regions are connected via an *n*-channel. This *n*-channel is connected to the Gate (G) via a thin insulating layer of SiO_2.

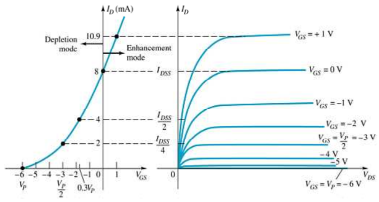
The *n*-doped material lies on a *p*-doped substrate that may have an additional terminal connection called Substrate (SS).



Basic MOSFET Operation

A depletion-type MOSFET can operate in two modes:

- **Depletion mode**
- **Enhancement mode**



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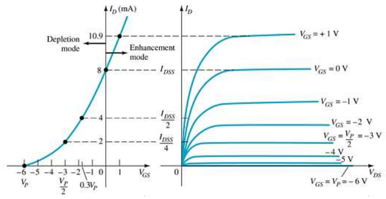
D-Type MOSFET in Depletion Mode

Depletion Mode

The characteristics are similar to a JFET.



- When $V_{GS} = 0$ V, $I_D = I_{DSS}$
- When $V_{GS} < 0$ V, $I_D < I_{DSS}$
- The formula used to plot the transfer curve still applies:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

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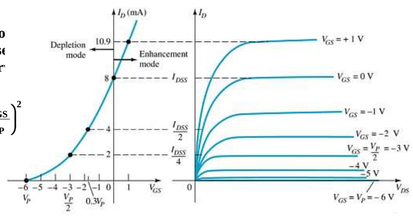
D-Type MOSFET in Enhancement Mode

Enhancement Mode

- $V_{GS} > 0$ V
- I_D increases abo
- The formula use the transfer cur applies:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



Note that V_{GS} is now a positive polarity

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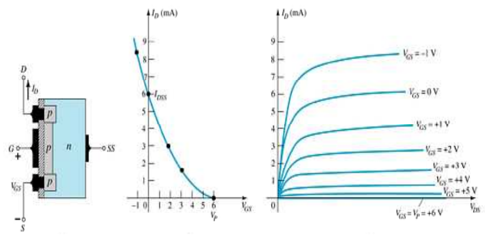
p-Channel D-Type MOSFET



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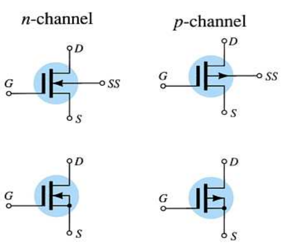
D-Type MOSFET Symbols



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Specification Sheet

Maximum Ratings

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage 2N3797	V_{DS}	20	Vdc
Gate–Source Voltage	V_{GS}	±10	Vdc
Drain Current	I_D	20	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	200 1.14	mW mW/°C
Junction Temperature Range	T_J	+175	°C
Storage Channel Temperature Range	T_{stg}	−65 to +200	°C

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Specification Sheet

Electrical Characteristics

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain Source Breakdown Voltage (V_{GS} = −7.0 V, I_D = 5.0 μA)	2N3797	$V_{(BR)DSX}$	20	25	–	Vdc
Gate Reverse Current (1) (V_{GS} = −10 V, V_{DS} = 0)		I_{GSS}	–	–	1.0	pAdc
(V_{GS} = −10 V, V_{DS} = 0, T_A = 150°C)			–	–	200	
Gate Source Cutoff Voltage (I_D = 2.0 μA, V_{DS} = 10 V)	2N3797	$V_{GS(off)}$	–	−5.0	−7.0	Vdc
Drain-Gate Reverse Current (1) (V_{DG} = 10 V, I_S = 0)		I_{DGO}	–	–	1.0	pAdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current (V_{DS} = 10 V, V_{GS} = 0)	2N3797	I_{DSS}	2.0	2.9	6.0	mAdc
On-State Drain Current (V_{DS} = 10 V, V_{GS} = +3.5 V)	2N3797	$I_{D(on)}$	9.0	14	18	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz)	2N3797	$\lvert y_{fs} \rvert$	1500	2300	3000	μmhos
(V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)	2N3797		1500	–	–	
Output Admittance (I_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz)	2N3797	$\lvert y_{os} \rvert$	–	27	60	μmhos
Input Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)	2N3797	C_{iss}	–	6.0	8.0	pF
Reverse Transfer Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	–	0.5	0.8	pF
FUNCTIONAL CHARACTERISTICS						
Noise Figure (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz, R_S = 3 megohms)		NF	–	3.8	–	dB

(1) This value of current includes both the FET leakage current as well as the leakage current associated with the test socket and fixture when measured under best attainable conditions.

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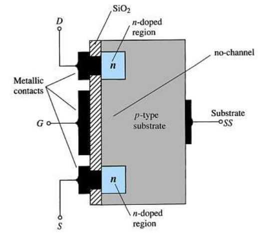
E-Type MOSFET Construction

- The **Drain** (D) and **Source** (S) connect to the to *n*-doped regions. These *n*-doped regions are connected via an *n*-channel
- The **Gate** (G) connects to the *p*-doped substrate via a thin insulating layer of SiO_2
- There is no channel
- The *n*-doped material lies on a *p*-doped substrate that may have an additional terminal connection called the **Substrate** (SS)



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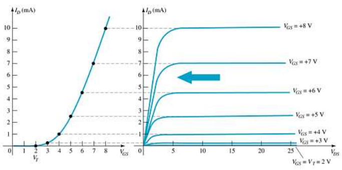
Basic Operation of the E-Type MOSFET

The enhancement-type MOSFET operates only in the enhancement mode.

- V_{GS} is always positive
- As V_{GS} increases, I_D increases
- As V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS}) and the saturation level, V_{DSsat} is reached



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E-Type MOSFET Transfer Curve

To determine I_D given V_{GS}:

$$I_D = k(V_{GS} - V_T)^2$$

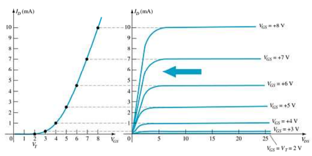
Where:
V_T = threshold voltage or voltage at which the MOSFET turns on

k, a constant, can be determined by using values at a specific point and the formula:

$$k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$

V_{DSsat} can be calculated by:

$$V_{Dsat} = V_{GS} - V_T$$



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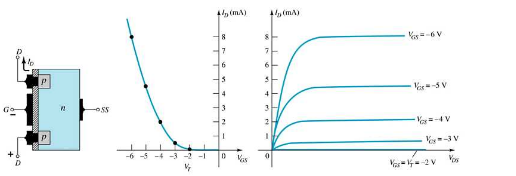
p-Channel E-Type MOSFETs



The *p*-channel enhancement-type MOSFET is similar to the *n*-channel, except that the voltage polarities and current directions are reversed.

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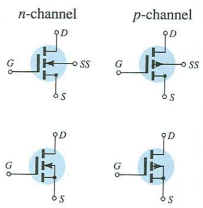
MOSFET Symbols



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Specification Sheet

Maximum Ratings

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	30	Vdc
Gate–Source Voltage*	V_{GS}	30	Vdc
Drain Current	I_D	30	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 1.7	mW mW/°C
Junction Temperature Range	T_J	175	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

* Transient potentials of ± 75 Volt will not cause gate-oxide failure.

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Specification Sheet

Electrical Characteristics

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (I_D = 10 μA, V_{GS} = 0)	$V_{(BR)DSX}$	25	–	Vdc
Zero-Gate-Voltage Drain Current (V_{DS} = 10 V, V_{GS} = 0) T_A = 25°C T_A = 150°C	I_{DSS}	– –	10 10	nAdc μAdc
Gate Reverse Current (V_{GS} = ± 15 Vdc, V_{DS} = 0)	I_{GSS}	–	± 10	pAdc
ON CHARACTERISTICS				
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 10μA)	$V_{GS(Th)}$	1.0	5	Vdc
Drain-Source On-Voltage (I_D = 2.0 mA, V_{GS} = 10V)	$V_{DS(on)}$	–	1.0	V
On-State Drain Current (V_{GS} = 10 V, V_{DS} = 10 V)	$I_{D(on)}$	3.0	–	mAdc
SMALL-SIGNAL CHARACTERISTICS				
Forward Transfer Admittance (V_{DS} = 10 V, I_D = 2.0 mA, f = 1.0 kHz)	$\|y_{fs}\|$	1000	–	μmho
Input Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 140 kHz)	C_{iss}	–	5.0	pF
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 0, f = 140 kHz)	C_{rss}	–	1.3	pF
Drain-Substrate Capacitance ($V_{D(SUB)}$ = 10 V, f = 140 kHz)	$C_{d(sub)}$	–	5.0	pF
Drain-Source Resistance (V_{GS} = 10 V, I_D = 0, f = 1.0 kHz)	$r_{ds(on)}$	–	300	ohms
SWITCHING CHARACTERISTICS (I_D = 2.0 mAdc, V_{DS} = 10 Vdc, (V_{GS} = 10 Vdc) (See Figure 9; Times Circuit Determined))				
Turn-On Delay (Fig. 5)	t_{d1}	–	45	ns
Rise Time (Fig. 6)	t_r	–	65	ns
Turn-Off Delay (Fig. 7)	t_{d2}	–	60	ns
Fall Time (Fig. 8)	t_f	–	100	ns

Handling MOSFETs

MOSFETs are very sensitive to static electricity. Because of the very thin SiO_2 layer between the external terminals and the layers of the device, any small electrical discharge can create an unwanted conduction.

Protection

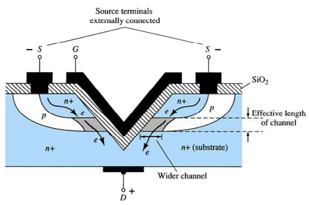
- Always transport in a static sensitive bag
- Always wear a static strap when handling MOSFETS
- Apply voltage limiting devices between the gate and source, such as back-to-back Zeners to limit any transient voltage.

VMOS Devices

VMOS (vertical MOSFET) increases the surface area of the device.

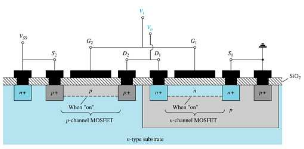
Advantages

- VMOS devices handle higher currents by providing more surface area to dissipate the heat.
- VMOS devices also have faster switching times.



CMOS Devices

CMOS (complementary MOSFET) uses a *p*-channel and *n*-channel MOSFET; often on the same substrate as shown here.



Advantages

- Useful in logic circuit designs
- Higher input impedance
- Faster switching speeds
- Lower operating power levels

Summary Table