COMP303 Computer Architecture

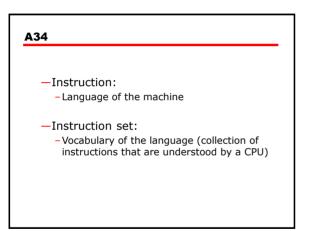
Some questions & answers

Prof. Nizamettin AYDIN, PhD <u>naydin@yildiz.edu.tr</u>

http://www.yildiz.edu.tr/~naydin

Q34

• What is an instruction and instruction set? Explain.

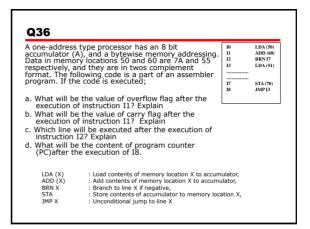


Q35

- Consider a stack-based processor with instructions
 PUSH, POP, ADD, SUB , MUL, and DIV.
- Write a program to compute

 $X = (A + B^2)/(D^2 - E)$

• X :	= (A + B ²)	/(D² – E)	
	PUSH A			
	PUSH B			
	PUSH B			
	MUL			
	ADD			
	PUSH D			
	PUSH D			
	MUL			
	PUSH E			
	SUB			
	DIV			
	POP X			



A36

a. Overflow flag is 1. - Both 7A and 55 are positive. But the result is negative: 7A (01111010) + 55 (01010101) CF (11001111) b. Carry flag will be 0, as there is no carry.

- c. Because the sign flag is 1 (the result is negative), instruction I7 will be executed after the execution of the instruction I2
- d. The program counter content will be I3

The contents of memory and		Memory	CPU reg	ister					
CPU registers of a computer	100	1240	101	PC					
system is given as following	101	5241	0003	A					
(the values are in hexadecimal).	102	2241	5241	IR					
What will be the actual operand	240	0003							
of the instruction for the;	241	0343							
 immediate addressing 	342	0003							
5	343	0302							
direct addressing									
indirect addressing									

A37			
a.	0241		
b.	0343		
c.	0302		
d.	0003		

Q38
 Assume a stack-based processor that includes the stack operations PUSH and POP. Arithmetic operations automatically involve the top one or two stack elements. Begin with an empty stack. What stack elements remain after the following instructions are executed?
PUSH 4
PUSH 7
PUSH 8
ADD
PUSH 10
SUB
MUL

A38		
Instruction PUSH 4	Stack (top on the left)	
	4	
PUSH 7		
	7,4	
PUSH 8	8, 7, 4	
ADD	0, 7, 4	
	(8+7=15), 4	
PUSH 10		
SUB	10, 15, 4	
500	(15-10=5), 4	
MUL	(// -	
	(5×4=20)	

Q39

 Compare zero-, one-, two-, and three-address machines by writing programs to compute X = (A + B × C)/(D - E × F) for each of the four machines (0 Address, 1 Address, 2 Address, 3 Address machines).

The instructions available for use are as follows:

0 Address	1 Address	2 Address	3 Address
PUSH M	LOAD M	MOV (X \leftarrow Y)	MOV (X \leftarrow Y)
POP M	STORE M	ADD $(X \leftarrow X + Y)$	ADD (X \leftarrow Y + Z)
ADD	ADD M	SUB (X \leftarrow X - Y)	SUB (X ← Y - Z)
SUB	SUB M	$MUL (X \leftarrow X \times Y)$	$MUL (X \leftarrow Y \times Z)$
MUL	MUL M	DIV $(X \leftarrow X / Y)$	DIV (X \leftarrow Y / Z)
DIV	DIV M		

A39 X = (A	+ B × C),	/(D – E × F)	
0 Address (Stack Machines) PUSH A PUSH B PUSH C MUL ADD PUSH D PUSH E PUSH F MUL SUB SUB DIV POP X	1 Address (Accumulator Machine) LOAD E MUL F STORE T LOAD D SUB T STORE T LOAD B MUL C ADD A DIV T STORE X	2 Address (Memory-Memory, or Register-register Machine) MOV R0, E MUL R0, F MUL R0, F MOV R1, D SUB R1, R0 MOV R0, B MUL R0, C ADD R0, A DIV R0, R1 MOV X, R0	3 Address Load-Store MUL R0, E, F SUB R0, D, R0 MUL R1, B, C ADD R1, A, R1 DIV X, R0, R1

Q40

- Assume a pipeline with 4 stages: —fetch instruction (FI),
 - -decode instruction and calculate addresses (DA),
 - -fetch operand (FO), and
 - -execute (EX).
- Draw the pipelinening diagram for a sequence of 7 instructions, in which the third instruction is a branch to instruction 15 that is taken and in which there are no dependencies.

	1	2	3	4	5	6	7	8	9	10		1	2	3	4	5	6	7	8	9
I1											I1	FI	DA	FO	EX					
I2											I2		FI	DA	FO	EX				
13											13			FI	DA	FO	ΕX			
I4											I4				FI	DA	FO			
15										+	15					FI	DA			
16						-		-		-	16						FI			
I15			-		-	+			-	-	I15							FI	DA	FC

Q41

- A pipelined processor has a clock rate of 2.5 GHz and executes a program with
 - 1.5 million instructions.
 - The pipeline has five stages, and instructions are issued at a rate of one per clock cycle.
 - Ignore penalties due to branch instructions and out-of-sequence executions.

What is the speedup of this processor for this program compared to a nonpipelined processor?

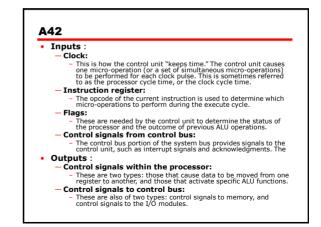
A41

We can ignore the initial filling up of the pipeline and the final emptying of the pipeline, because this involves only a few instructions out of 1.5 million instructions.

Therefore the speedup is a factor of five.

Q42

 Provide a typical list of the inputs and outputs of a control unit.



Q43

- Your ALU can add its two input registers, and it can logically complement the bits of either input register, but it cannot subtract.
- Numbers are to be stored in two's complement representation.
- List the micro-operations your control unit must perform to cause a subtraction.

A43

• Consider the instruction SUB R1, X, which subtracts the contents of location X from the contents of register R1, and places the result in R1.

•	t1:	MAR \leftarrow	(IR(address))
•	t2:	MBR \leftarrow	Memory
•	t3:	MBR \leftarrow	Complement(MBR)
•	t4:	MBR \leftarrow	Increment(MBR)
•	t5:	R1 ←	(R1) + (MBR)