COMP303
Computer Architecture

Some questions & answers

Prof. Nizamettin AYDIN, PhD
naydin@yildiz.edu.tr

http://www.yildiz.edu.tr/~naydin

Q10

A computer system has an 8 bit accumulator and 12 bit address bus.

If the content of memory location 1F0 is the binary number 11000011;

(a) what is the corresponding decimal value when the number represents an unsigned integer number?

(b) what is the corresponding decimal value when the number represents a twos complement number?

(c) what is the corresponding decimal value when the number represents a ones complement number?

(d) Assuming that the most significant bit is parity bit, what is the corresponding letter when the number represents an ASCII character (hint: ASCII character is represented by 7 bits and 41H represents A)?

A10

Binary 11000011:

(a) $1\times2^7+1\times2^6+1\times2^1+1\times2^0 = 195$

(b) $-1\times2^7+1\times2^6+1\times2^1+1\times2^0 = -61$

(c) -60

(d) If the most significant bit is parity bit, ASCII character represented by 1000011 is 100 0011 (43 in hexadecimal) corresponding to capital letter C.

Q11

Consider a dynamic RAM that must be given a refresh cycle 64 times per ms.

—Each refresh operation requires 150 ns;

What percentage of the memory's total operating time must be given to refreshes?

A11

- In 1 ms, the time devoted to refresh is:
  64 × 150 ns = 9600 ns = 9.6 μs
  =0.0096 ms.
- The fraction of time devoted to memory refresh is:
  $(9.6 \times 10^{-6}\ s)/10^{-3}\ s = 0.0096$,
  which is 0.96%.

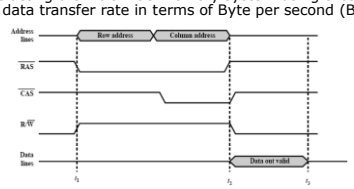
Q12

- Following figure shows a simplified timing diagram for a DRAM read operation over a bus.
- The access time is considered to last from t_1 to t_2. Then there is a recharge time, lasting from t_2 to t_3, during which DRAM chips will have to recharge before the processor can access them again.

a. Assume that the access time is 60 ns and the recharge time is 40 ns. What is the memory cycle time?

b. What is the maximum data rate this DRAM can sustain, assuming a 1-bit output?

c. Constructing a 32-bit wide memory system using these chips yields what data transfer rate in terms of Byte per second (B/s)?



A12

a. Memory cycle time = 60 + 40 = 100 ns.

b. The maximum data rate is 1 bit every 100 ns, which is 10 Mb/s.

c. 32×10 Mbps = 320 Mbps
= 320 Mbps / 8 = 40 MB/s.

Q13

In the Intel 8088 microprocessor, a bus read operation requires four processor clock cycles.

Assuming a processor clock rate of 8 MHz (fc = 8 Mega Hertz);

a. what is the maximum data transfer rate? (Data transfer rate is the total number of bytes transferred in one second)

b. what is the maximum data transfer rate if a one clock cycle wait state is inserted per byte transferred? (In wait state processor does nothing)

A13

a. The clock period is Tcc = 1/fc = 1/8 MHz
$=125 \text{ ns} = 125\times10^{-9}$ s

One bus read cycle is Tbc = 4×Tcc = 4×125
=500 ns = 0.5 μs.

If the bus cycles repeat one after another;

maximum data transfer rate is $1/(0.5\times10^{-6})$ = 2×10^{6} Byte per second = 2 MB/s.

b. The wait state extends the bus read cycle by 125 ns, for a total duration of 0.625 μs.

The corresponding data transfer rate is 1/0.625 = 1.6 MB/s.

Q14

- If one line of an assembler program (which loads contents of memory location 940 to the accumulator) for a hypothetical processor and corresponding machine code is given as:

address	assembler	machine code	
300	lda 940	1940	(the values are in hexd.)

a. How many bits are needed for the program counter?

b. How many bits are needed for the instruction register?

c. What is the maximum directly addressable memory capacity in KBytes?

d. For the memory location 940, find the Tag, Line, and Word values in hexadecimal format for a direct-mapped cache, when tag-id=4 bits, line-id=6 bits, word-id=2 bits.

A14

a. Because the address size is 3 nibbles (3x4=12 bits), a 12 bit Program Counter is required.

b. Instruction register size equals to *op-code size* + *address size*(4+12), which is 16 bits.

c. Maximum memory capacity = 2^{12} bytes = 2^{10+2} bytes = $2^2\times2^{10}$ bytes = 4 Kbytes

d. First, write the address in binary format:
$(940)_{16} = (1001\ 0100\ 0000)_2$
Then define the Tag, Line, and Word values:
Tag-id← 100101000000 →Word-id
Line-id
Tag-id = 1001 = 9
Line-id = 00010000 = 10
Word-id = 0000 = 0

Q15

Given the hexadecimal main memory address A1F85B73;

a. How many bits are needed for the program counter?

b. How many bits are needed for the instruction register if op-code is 8 bits.

c. What is the maximum directly addressable memory capacity in GByte?

d. Find the Tag, Line, and Word values in hexadecimal format for a direct-mapped cache, when *tag-id*=13 bits, *line-id*=16 bits, *word-id*=3 bits.

A15

a. Because the address size is 4 bytes (32 bits), a 32 bit Program Counter is required.

b. Instruction register size equals to *op-code size* + *address size*, which is 40 bits.

c. Maximum memory capacity = 2^{32} bytes = 2^{30+2} bytes = $2^2 \times 2^{30}$ bytes = 4 Gbytes

d. First, write the address in binary format:
1010 0001 1111 1000 0101 1011 0111 0011
Then define the Tag, Line, and Word values:

Tag-id← 10100001111110000101101101110011 →Word-id
Line-id

Tag-id = 0001010000111111 = 143F
Line-id = 0000101101101110 = 0B6E
Word-id = 0011 = 3

Q16

Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes.

Assume that a direct mapped cache consisting of 32 lines is used with this machine.

a. How is the memory address divided into tag, line number, and byte number?

b. Into what line would bytes with each of the following addresses be stored?
   i. 0001 0001 0001 1011
   ii. 1100 0011 0011 0100

A16

a. Address size is 16 bits
word-id= $\log_2$(block size) = $\log_2(8)$ = 3 bits
line-id = $\log_2$(#of lines) = $\log_2(32)$ = 5 bits
tag-id = 16 – (5+3) = 8 bits

b. i. 00010001 00011 011 ➔ line id = 03
ii. 11000011 00110 100 ➔ line id = 06