COMP303
Computer Architecture

Some questions & answers

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Q1

- What are the four main components of any general-purpose microprocessor?

A1

—A **memory (register)**,
- which stores both data and instructions:

—An **arithmetic and logic unit** (ALU)
- capable of operating on binary data;

—A **control unit**,
- which interprets the instructions in memory and causes them to be executed;

—**Input and output (I/O) equipment**
- operated by the control unit.

Q2

- At the integrated circuit level, what are the three principal constituents of a computer system?

A2

—Gates,

—Memory cells

—Interconnections among gates and memory cells

Q3

- List and explain the key characteristics of a computer family.

A3

- **Similar or identical instruction set**
  - In many cases, the same set of machine instructions is supported on all members of the family. Thus, a program that executes on one machine will also execute on any other.
- **Similar or identical operating system**
  - The same basic operating system is available for all family members.
- **Increasing speed**
  - The rate of instruction execution increases in going from lower to higher family members.
- **Increasing Number of I/O ports**
  - In going from lower to higher family members.
- **Increasing memory size**
  - In going from lower to higher family members.
- **Increasing cost**
  - In going from lower to higher family members.

Q4

- Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields:

  The first byte contains the opcode and the remainder the immediate operand or an operand address.
  - a. What is the maximum directly addressable memory capacity (in bytes)?
  - b. How many bits are needed for the program counter and the instruction register?

A4

a. Address field of the instruction is 24 bits.

- Therefore the total memory capacity is $2^{24} = 2^4 \times 2^{20} = 16$ Mbytes
  - (2^{20} is 1 Mega)

b. Because the address field of the instruction is 24 bits,

- The program counter must be at least 24 bits.
- If the instruction register is to contain the whole instruction, it will have to be 32-bits long

Q5

Consider a 32-bit microprocessor, with a 16-bit external data bus, driven by an 8-MHz input clock.

Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles.

- What is the maximum data transfer rate that this microprocessor can sustain?

A5

- Clock cycle = 1/Clock frequency
  Clock cycle = 1/8 MHz = 0.125×10^{-6} s
  $= 125 \times 10^{-9}$ s = 125 ns

- Bus cycle = number of clocks x Clock cycle
  Bus cycle = 4 x 125 ns = 500 ns

- 2 bytes transferred every 500 ns; thus

- transfer rate = $2/(500 \times 10^{-9}) = 2/(5 \times 10^{-7})$
  $= 0.4 \times 10^7 = 4$ MBytes/sec

Q6

An 8 bit microprocessor system has 9 address lines to address relevant memory locations.

a. Assuming that the data size is 1 byte, what is the address of the last memory location?

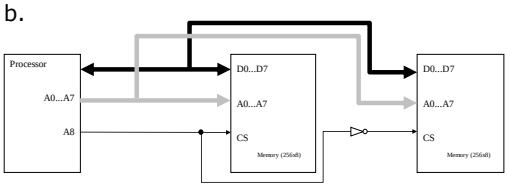
b. Design the required memory system using memory chips organized as 256x8 bits.

A6

a. Because the processor has 9 address lines the total directly addressable memory size is $2^9 = 512$ Bytes.

So, the address of the last memory location will be **2^9-1 = 511**

b.



Q7

A computer system has the following floating point format:

1 bit sign 5 bits biased exponent 10 bits mantissa

(bias can be taken as $2^{(\text{number of bits in exponet}-1)}-1$)

—If the given number is 19.75, determine the following values:

—a. Corresponding binary number
—b. Corresponding hexadecimal number
—c. Corresponding 16 bit floating point number

A7

a. $(19.75)_{10} = (10011.11)_2$
b. $(19.75)_{10} = (0001\ 0011.1100)_2 = (13.C)_{16}$
c. $(19.75)_{10} = (10011.11)_2 \Rightarrow (1.001111\times2^{00100})$
biased exponential format= $(1.001111\times2^{00100+01111})$
biased exponential format = $(1.001111\times2^{10011})$

S = 0, BE = 10011, M = 0011110000

$(19.75)_{10}=(0\ 10011\ 0011110000)_{float}$

Q8

- A given microprocessor has words of one byte.

What is the smallest and largest integer that can be represented in the following representation?

a. Unsigned
b. Sign magnitude
c. Ones complement
d. Twos complement
e. Binary coded decimal

A8

The word size is 1 byte (8 bits). So,

a. 0; 255

b. –127; 127

c. –127; 127

d. –128; 127

e. 00; 99

Q9

- In a signed (2s complement number system) addition, if the "carry in" and the "carry out" of the sign bit differ, there is an overflow.

a. Determine whether there is an overflow in the following operations or not. (use 4 bit 2s complement numbers)
4+3; -7-6; 5+7; -3-2
b. Design a circuit that whenever an overflow happens the output becames 1, otherwise 0.

A9.a

- If the "carry in" and the "carry out" of the sign bit differ, there is an overflow.

operation		4+3		-7-6		5+7		-3-2
Carry in		0		0		1		1
		0100		1001		0101		1101
	+	0011	+	1010	+	0111	+	1110
Result		0111		0011		1100		1011
Cary out	0		1		0		1	
overflow		no		yes		yes		no

A9.b

Truth table:

C_i	C_o	F
0	0	0
0	1	1
1	0	1
1	1	0

Overflow function:
$F=C_i' C_o+C_i C_o'=C_i \oplus C_o$

Implementation: