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2nd Midterm Exam (25.12.2007)

CSE2201(2204)- Computer Organization

1. Classify and describe registers that a CPU consists of. *(20 pts)*

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2. x = 100 and y = 110 are two unsigned integer numbers.
   Compute the product p = x × y using multiplication algorithm? *(20 pts)*

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3. Consider an array of five drives (X0, X1, X2, X3 contain data, **X4** is parity disk). *(15 pts)*
   Parity of *i*th bit is calculated as X4(*i*) = X3(*i*) ⊕ X2(*i*) ⊕ X1(*i*) ⊕ X0(*i*)
   Suppose that drive **X2** has failed. Show how to regenerate the contents of **X2.**

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4. A one-address type processor has an 8 bit accumulator (A), and a bytewise memory addressing. Data in memory locations 20 and 30 are FA and A5 respectively, and they are in twos complement format. The following code is a part of an assembler program. If the code is executed;

I0	**LDA (20)**
I1	**ADD (30)**
I2	**BRN I7**
I3	**LDA (51)**
.....	
.....	
I7	**STA (70)**
I8	**JMP I3**

   (a) What will be the value of overflow flag after the execution of instruction I1? Explain *(5 pts)*
   (b) What will be the value of carry flag after the execution of instruction I1? Explain *(5 pts)*
   (c) Which line will be executed after the execution of instruction I2? Explain *(5 pts)*
   (d) What will be the content of program counter (PC) after the execution of I8. *(5 pts)*

   LDA (X): *Load contents of memory location X to accumulator*
   ADD (X): *Add contents of memory location X to accumulator*
   BRN X: *Branch to line X if negative*
   STA: *Store contents of accumulator to memory location X*
   JMP X: *Unconditional jump to line X*

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5. A particular system is controlled by an operator through commands entered from a keyboard. Suppose the processor scans the keyboard every 100 ms. How many times will the keyboard be checked in an 8-hour period? *(10 pts)*

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6. (a) Classify external devices to be connected to a computer system *(5 pts)*
   (b) Write principle I/O techniques used in a computer system *(5 pts)*

1.

a. **User-visible register:** A User-Visible Register is one that may be referenced by means of the machine language that the CPU executes.

General purpose,
Data,
Address,
Condition codes (flags)

b. **Control and status registers:** Registers that are employed to control the operation of the CPU.

Program Counter (PC)
Instruction Register (IR)
Memory Address Register (MAR)
Memory Buffer Register (MBR)

2.

If Q = 100 and M = 110, then the solution:

	C	A	Q	M	Process
	0	000	100	110	Initial
Step 1	0	000	010	110	Logic Shift Right
Step 2	0	000	001	110	Logic Shift Right
Step 3	0	110	001	110	A ← A + M
	0	011	000	110	Logic Shift Right

The following solution is also correct:

	C	A	Q	M	Process
	0	000	110	100	Initial
Step 1	0	000	011	100	Logic Shift Right
Step 2	0	100	011	100	A ← A + M
	0	010	001	100	Logic Shift Right
Step 3	0	110	001	100	A ← A + M
	0	011	000	100	Logic Shift Right

$p = x \times y = 100 \times 110 = (011000)_2 = (24)_{10}$

3.

The contents of X2 can be regenerated by XORing both sides by X4 and X2 :

$X2(i) \oplus X4(i) \oplus X4(i) = X3(i) \oplus X2(i) \oplus X1(i) \oplus X0(i) \oplus X2(i) \oplus X4(i)$

Because $X4(i) \oplus X4(i) = 0$ and $X2(i) \oplus X2(i) = 0$;

$X2(i) = X4(i) \oplus X3(i) \oplus X1(i) \oplus X0(i)$

4.

```
                 11
    FA        (11111010)
+   A5        (10100101)
    9F      1 (10011111)
```

(a) Overflow flag is 0.
Both FA and A5 are negative, and the result is also negative (or carry-in and carry-out are the same).

(b) Because the carry-out is 1, carry flag will be 1.

(c) Because the sign flag is 1 (the result is negative), instruction I7 will be executed after the execution of the instruction I2

(d) The program counter content will be I3

5.

in 100×10^{-3} s 1 scan
in 1 s x scan

$x = 1/(100\times10^{-3}) = 1000/100 = 10$ scan

So, the processor scans the keyboard 10 times per second.

1 hour = 60×60 s = 3600 s

In 8 hours, the number of times the keyboard is scanned is $10 \times 8 \times 3600 = 288000$.

6.

(a) Human readable (screen, printer, keyboard, etc),
Machine readable (for monitoring and control)
Communication (modem, Network Interface Card (NIC), etc)

(b) Programmed I/O (reserves a register for each I/O device. Each register is continually polled to detect data arrival)
Interrupt-Driven I/O (allows the CPU to do other things until I/O is requested)
Direct Memory Access (DMA) (offloads I/O processing to a special-purpose chip that takes care of the details)
Channel I/O (uses dedicated I/O processors)