Name-surname : **Signature:**
Student no :

1st Midterm Exam (23.11.2005)

CSE 2201- Computer Organization

1(10). What are the main components of any general-purpose computer?

CPU, memory, Input/Output, System interconnection

2(10). Perform the following conversions:

a. $(204.125)_{10}$ = (…….)$_{16}$ b. 196 = (…….)$_{BCD}$

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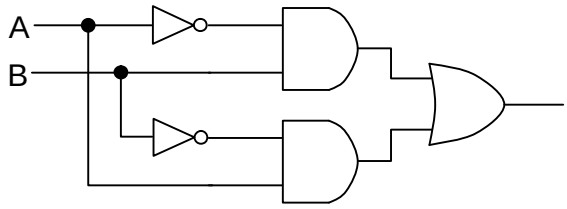
a. $(204.125)_{10} = (11001100.001)_2 = (CC.2)_{16}$ b. 196 = $(0001\ 1001\ 0110)_{BCD}$

3(10). Construct the operation XOR using the basic Boolean operations AND, OR, and NOT.

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

$F = \overline{A}B + A\overline{B}$



4(10). Classify the memory system in a computer.

Registers, L1 Cache, L2 Cache, Main memory, Disk cache, Disk, Optical, Tape

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5(10). List the possible states that define an instruction cycle.

Instruction address calculation (iac): Determine the address of the next instruction to be executed.

Instruction fetch (if): Read instruction from its memory location into the processor.

Instruction operation decoding (iod): Analyze instruction to determine type of operation to be performed and operand(s) to be used.

Operand address calculation (oac): If the operation involves reference to an operand in memory or available via I/O, then determine the address of the operand.

Operand fetch (of): Fetch the operand from memory or read it in from I/O.

Data operation (do): Perform the operation indicated in the instruction.

Operand store (os): Write the result into memory or out to I/O.

6(10). List and briefly define three techniques for performing I/O in a computer.

Programmed I/O: The processor issues an I/O command, on behalf of a process, to an I/O module; that process then busy-waits for the operation to be completed before proceeding.

Interrupt-driven I/O: The processor issues an I/O command on behalf of a process, continues to execute subsequent instructions, and is interrupted by the I/O module when the latter has completed its work. The subsequent instructions may be in the same process, if it is not necessary for that process to wait for the completion of the I/O. Otherwise, the process is suspended pending the interrupt and other work is performed.

Direct memory access (DMA): A DMA module controls the exchange of data between main memory and an I/O module. The processor sends a request for the transfer of a block of data to the DMA module and is interrupted only after the entire block has been transferred.

7(20). Given the hexadecimal main memory address A1F85B73;

a. How many bits are needed for the program counter?

b. How many bits are needed for the instruction register if op-code is 8 bits.

c. What is the maximum directly addressable memory capacity in Gbyte (Giga byte)?

d. Find the Tag, Line, and Word values in hexadecimal format for a direct-mapped cache, when *tag-id*=13 bits, *line-id*=16 bits, *word-id*=3 bits.

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a. Because the address size is 4 bytes (32 bits), a 32 bit Program Counter is required.

b. Instruction register size equals to *op-code size* + *address size*, which is 40 bits.

c. Maximum memory capacity = 2^{32} bytes = 2^{30+2} bytes = $2^2 \times 2^{30}$ bytes = 4 Gbytes

d. First, write the address in binary format: 1010 0001 1111 1000 0101 1011 0111 0011

Then define the Tag, Line, and Word values:

Tag-id← 1010000111111000010110110111 0011 →Word-id

Line-id

Tag-id = 0001010000111111 = 143F

Line-id = 0000101101101110 = 0B6E

Word-id = 0011 = 3

8(20). Given the memory contents of IAS computer shown below

Address	Contents
08A	010FA210FB
08B	010FA0F08D
08C	020FA210FB

a. Show the assembly language code for the program, starting at address 08A.

b. Write the assembly language code that does the following calculation. (Assume that *A*, *B*, and *C* are stored in the memory locations 100, 200, and 300 respectively)

$C = (A^2/B)$

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a.

Address	**Contents**
08AL	LOAD M(0FA)
08AR	STOR M(0FB)
08BL	LOAD M(0FA)
08BR	JUMP +M(08D,0:19)
08CL	LOAD –M(0FA)
08CR	STOR M(0FB)
08D	

b.

Address	**Contents**	**Explanation**
000L	LOAD M(Q), M(100)	Transfer contents of memory location 100 to MQ
000R	MUL M(100)	A^2 : multiply MQ with contents of memory location 100
001L	DIV M(200)	A^2/B: divide AC with contents of memory location 200
001R	LOAD M(Q)	Transfer contents of MQ to AC
002L	STOR M(300)	Store contents of AC to memory location 300
002R	JUMP M(002,20:39)	Halt : terminate the program