Name-surname : **Signature:**
Student no :

2nd Midterm Exam (28.12.2005)

**********CSE 2201(2204) - Computer Organization**********

1(10). What basic tasks a control unit performs?

Sequencing: *The control unit causes the processor to step through a series of micro-operations in the proper sequence, based on the program being executed.*

Execution: *The control unit causes each micro-operation to be performed.*

2(10). A microprocessor is clocked at a rate of 5 GHz. (f= 5 GHz)

a. How long is a clock cycle?

T = 1/f = 1/5 GHz = 0.2 ns

b. What is the duration of a particular machine instruction consisting of 4 clock cycles?

4´0.2 = 0.8 ns

3(20). In a computer system, address 5 contains 100; address 100 contains decimal value 4. What would be the contents of accumulator after running the following assembler code. Explain what happens. (Assume that all valuas are decimal).

```
1  LOAD IMMEDIATE 4
2  SHIFTL
3  MUL DIRECT 100
4  ADD INDIRECT 5
5  SHIFTR
```

1	*Content of AC becomes 4 .*	*AC= 4*
2	*Content of AC is multiplied by 2.*	*AC = 8*
3	*Content of AC is multiplied by the content of memory location 100, which is 4.*	*AC=32*
4	*Content of memory location 100, which is referred by the memory location 5 is added to AC.*	*AC=36*
5	*Content of AC is divided by 2.*	*AC=18*

4(20).

a. Describe what an instruction set is.

The complete collection of instructions that are understood by a CPU.

b. List the elements of an instruction.

Operation code (Op code), Source Operand reference, Result Operand reference, Next Instruction reference.

c. What type of instructions a processor have. Give one example for each type.

Data processing (add); Data storage (load); Data movement (I/O) (in); Program flow control (jump)

d. List the registers that are essential to instruction execution.

Program Counter (PC); Instruction Register (IR); Memory Address Register (MAR); Memory Buffer Register (MBR)

5(20). Perform the following operations:

a. Subtract 5 from 20 in twos complement arithmetic (use 8 bits to express in binary).

00010100-00000101 = 00010100+11111011*(twos complement of* 00000101*)*= 1 00001111 *(ignore overflow)*

b. Find 11001100-101110 using twos complement arithmetic.

11001100 *(-52)*	11001100	11001100
- 101110 *(-18)*	- 11101110 *(sign extended)*	+ 00010010 *(twos complement of* 11101110*)*
(-34)		11011110 *(-34 in twos complement)*

c. Binary number "0 10000000 10000000000000000000000" uses IEEE 32-bit floating point format. What is the equivalent decimal value? (reminder: $N=(-1)^s \times 1.\text{fraction} \times 2^{(\text{biased exp}-127)}$)

0 10000000 10000000000000000000000

Sign bit *Biased exponent* *Fraction*

s = 0

1.fraction = $(1.10000000000000000000000)_2 = (1.5)_{10}$

biased exp = $(10000000)_2=(128)_{10}$

$N = (-1)^s \times 1.\text{fraction} \times 2^{(\text{biased exp}-127)} = (-1)^0 \times 1.5 \times 2^{(128-127)} = 1.5 \times 2^1 = 1.5 \times 2 = 3$

d. Two numbers both having the same sign were added. The result has the opposite sign. What happened?

An overflow happened

6(20). Given x = 0100 and y = 1100 in twos complement notation (i.e., x = 4, y = -4), compute the product p = x × y with Booth's algorithm.

A	Q	Q_{-1}	M	Process
0000	1100	0	0100	Initial
0000	0110	0	0100	Shift
0000	0011	0	0100	Shift
1100	0011	0	0100	A ← A – M
1110	0001	1	0100	Shift
1111	0000	1	0100	Shift

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Execution: *The control unit causes each micro-operation to be performed.*

2(10). A microprocessor is clocked at a rate of 4 GHz. (f= 4 GHz)

a. How long is a clock cycle?

T = 1/f = 1/4 GHz = 0.25 ns

b. What is the duration of a particular machine instruction consisting of 4 clock cycles?

4´0.25 = 1 ns

3(20). In a computer system, address 5 contains 100; address 100 contains decimal value 8. What would be the contents of accumulator after running the following assembler code? Explain what happens. (Assume that all values are decimal).

1 LOAD IMMEDIATE 4
2 SHIFTR
3 MUL DIRECT 100
4 ADD INDIRECT 5
5 SHIFTL

1	*Content of AC becomes 4 .*	*AC= 4*
2	*Content of AC is divided by 2.*	*AC = 2*
3	*Content of AC is multiplied by the content of memory location 100, which is 8.*	*AC=16*
4	*Content of memory location 100, which is referred by the memory location 5 is added to AC.*	*AC=24*
5	*Content of AC is multiplied by 2.*	*AC=48*

4(20).

a. List the registers that are essential to instruction execution.
Program Counter (PC); Instruction Register (IR); Memory Address Register (MAR); Memory Buffer Register (MBR)

b. What type of instructions a processor have. Give one example for each type.
Data processing (add); Data storage (load); Data movement (I/O) (in); Program flow control (jump)

c. Describe what an instruction set is.
The complete collection of instructions that are understood by a CPU.

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Operation code (Op code), Source Operand reference, Result Operand reference, Next Instruction reference.

5(20).

a. Two numbers both having the same sign were added. The result has the opposite sign. What happened?
An overflow happened

b. Subtract 4 from 21 in twos complement arithmetic (use 8 bits to express in binary).
00010101-00000100 = 00010101+11111100*(twos complement of* 00000100*)*= 1 00010001 *(ignore overflow)*

c. Find 11001100-101010 using twos complement arithmetic.

11001100 *(-52)*	11001100	11001100
- 101010 *(-22)*	- 11101010 *(sign extended)*	+ 00010110 *(twos complement of* 11101010*)*
(-30)		11100010 *(-30 in twos complement)*

d. Binary number "1 10000000 10000000000000000000000" uses IEEE 32-bit floating point format. What is the equivalent decimal value? (reminder: $N=(-1)^s \times 1.\text{fraction} \times 2^{(\text{biased exp}-127)}$)

1 10000000 10000000000000000000000
Sign bit *Biased exponent* *Fraction*

s = 1
1.fraction = $(1.10000000000000000000000)_2 = (1.5)_{10}$
biased exp = $(10000000)_2=(128)_{10}$
$N = (-1)^s \times 1.\text{fraction} \times 2^{(\text{biased exp}-127)} = (-1)^1 \times 1.5 \times 2^{(128-127)} = -1.5 \times 2^1 = -1.5 \times 2 = -3$

6(20). Given x = 0101 and y = 1100 in twos complement notation (i.e., x = 5, y = -4), compute the product p = x × y with Booth's algorithm. (Complete the following table)

A	Q	Q_{-1}	M	Process
0000	1100	0	0101	Initial
0000	0110	0	0101	Shift
0000	0011	0	0101	Shift
1011	0011	0	0101	A ← A – M
1101	1001	1	0101	Shift
1110	1100	1	0101	Shift